What is claimed is:

[Claim 1] A method comprising:

providing a first layout database of an integrated circuit design, wherein the first layout database is obtained before optical proximity correction treatment;
providing a second layout database of the integrated circuit design, wherein the second database is obtained after optical proximity correction treatment;
finding a location of a first structure in the first layout database;
finding the first structure in the second layout database based on its location in the first layout database;
simulating a resulting layout output for the first structure using the second layout database;
measuring a first critical dimension of the first structure from the resulting layout output for the first structure;
comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database; and
flagging the first structure in the second database if the first critical dimension is less than the first drawn dimension in the first database.

[Claim 2] The method of claim 1 wherein the step of flagging the first structure in the second database if the first dimension is less than the first drawn dimension in the first database is replaced by flagging the first structure in the second database if the first dimension is less than the first drawn dimension plus a tolerance value in the first database.

[Claim 3] The method of claim 2 wherein the tolerance value defined by a user.

[Claim 4] The method of claim 1 wherein the first and second layout databases in GDSII format.

[Claim 5] The method of claim 1 wherein the first structure is at least one of a transistor gate, transistor end-cap, line, line-end, via and gap, or contact and gap.

[Claim 6] The method of claim 1 wherein the step of finding a location of a first structure in the first layout database is performed using pattern recognition.

[Claim 7] The method of claim 1 wherein when the first structure is a transistor gate, the first critical dimension is a gate length.

[Claim 8] The method of claim 1 wherein when the first structure is a transistor gate, the first critical dimension is a gate width.

[Claim 9] The method of claim 1 further comprising:

building a model of a process, to be used to fabricated the integrated circuit design, and wherein the step of simulating a resulting layout output for the first structure using the second layout database is performed using this model of the process.

[Claim 10] The method of claim 1 where the step of simulating a resulting layout output for the first structure using the second layout database comprises consulting a look-up table.

[Claim 11] A method executing in a computer-aided design system for designing circuitry prior to physical implementation, wherein the method checks compliance of a simulated layout output of a selected structure provided in a first database of a integrated circuit design after optical proximity correction treatment to a drawn dimension the selected structure provided in a second database of the integrated circuit design before optical proximity correction treatment, the method comprising:

providing a design rule that is violated when a measured critical dimension of the simulated layout output for the selected structure is less than the drawn dimension of the selected structure;
applying the design rule to at least a portion of the integrated circuit design; and
providing a user-discernable indication of any violation of the design rule.

[Claim 12] The method of claim 11 wherein the selected structure is at least one of a transistor gate, transistor end-cap, line, line-end, via and gap, or contact and gap.

[Claim 13] The method of claim 11 wherein the step of providing a design rule that is violated when a measured critical dimension of the simulated layout output for the selected structure is less than the drawn dimension of the selected structure is replaced by the step of providing a design rule that is violated when a measured critical dimension of the simulated layout output for the selected structure is less than the drawn dimension of the selected structure plus a tolerance value.

[Claim 14] The method of claim 13 wherein the tolerance value is specified by a user.

[Claim 15] A method comprising:

providing a first layout database of an integrated circuit design, wherein the first layout database is obtained before optical proximity correction treatment;
providing a second layout database of the integrated circuit design, wherein the second database is obtained after optical proximity correction treatment;
finding a location of a first structure in the first layout database;
finding the first structure in the second layout database based on its location in the first layout database;
simulating a resulting layout output for the first structure using the second layout database;
measuring a first critical dimension of the first structure from the resulting layout output for the first structure;

comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database; and
flagging the first structure in the first database if the first critical dimension is less than the first drawn dimension in the first database.

[Claim 16] The method of claim 15 further comprising:

flagging the first structure in the second database if the first critical dimension is less than the first drawn dimension in the first database.